

REMARKS

Claims 1, 5, 7 and 8 have been amended to clarify the invention, and to better define the invention over the prior art. Specifically, the claim language “minimum processing dimension” has been replaced with “half pitch.” The original Specification has been amended to correct grammatical errors, employ more idiomatic English and to clarify the invention. No new matter has been added by any of the aforementioned changes.

Turing to the art rejections, the rejection of claims 1 and 2 as being anticipated by Uchida et al. or by Hidaka et al. is in error. Claim 1, as amended, requires “[a] gate length of said gate electrode is longer than a half pitch.” Neither Uchida et al. nor Hidaka et al. teach this feature.

Uchida et al. teaches, to decrease the variation in the characteristics of the transistor, forming the gates of the MISFET longer than a minimum processable size, i.e. longer than 2 μm (Column 7, lines 45-47; column 12, lines 4-17). Hidaka et al. teaches forming a gate length longer than the minimum design dimension, i.e. longer than 0.20 microns (Column 2, lines 26-29; column 4, lines 25-32). However, neither of these references teach setting the length of the gate electrode in relation to the half pitch. Both require dimensions of the gate electrode larger than some arbitrary absolute value and neither teach a length of the gate electrode in relation to the half pitch. Thus, claims 1 and 2 are not anticipated or for that matter rendered obvious by Uchida et al. or Hidaka et al.

The Examiner’s rejection of claims 3 and 4 under 35 USC §103(a) as being unpatentable over Applicants’ Admitted Prior Art (AAPA) in view of Bronner et al. (US Patent No. 6,767,789) also is in error. Claims 3 and 4 indirectly depend on independent claim 1.

Neither AAPA nor Bronner et al. teach a gate length of the gate electrode longer than the half pitch. AAPA teaches a gate length equal to or less than the half pitch. Bronner et al. fails to provide the missing teachings of the AAPA. Bronner et al. teaches forming a gate longer than some absolute unspecified minimum dimension (Column 2, lines 50-58).

Furthermore, Bronner et al. actually teaches away from using a gate longer than a minimum dimension. Bronner et al. states a longer gate length "makes it almost impossible to effectively reduce the size of the DRAM cell." (Column 2, lines 50-58) and therefore Bronner et al. teaches away from Applicants' invention. Thus, claims 1 and 4 are patentable over the combination of AAPA and Bronner et al.

Similar comments apply to the rejection of claims 5 and 6. Claims 5 and 6 are indirectly dependent on claim 1. The deficiency of the AAPA combined with Bronner et al. are discussed above with respect to the rejection of claims 3 and 4. Thus, claims 5 and 6 are patentable for the same reasons above adduced relative to claim 1, as well as for their own additional limitations (35 USC §112). Accordingly, the rejection of claims 5 and 6 is likewise in error.

Finally, turning to the rejection of claims 7 and 8 as being obvious from Hidaka et al., claims 7 and 8 are both directly dependent on claim 1. The deficiencies of Hidaka et al. vis-à-vis claim 1 are discussed above. Thus, claims 7 and 8 are patentable over Hidaka et al. for the same reasons above adduced relative to claim 1 as well as for their own additional limitations (35 USC §112).

In rejecting claims 7 and 8, the Examiner posits Hidaka et al. disclose the invention except for the impurity concentration or the exact gate length. However, the Examiner claims

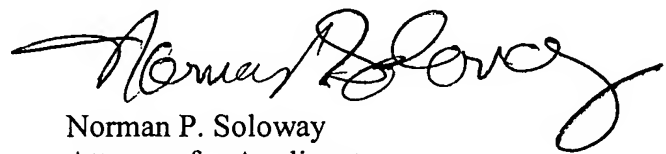
it would be obvious over Hidaka et al. because “[i]t has been held that the general condition of a claim is disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art” (Cipher 8, paragraph 2).

However, a particular parameter must be recognized as a result-effective variable before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. In re Antonie, 559 F.2d 618, 195 USPQ 6 (CCPA 1977). Hidaka et al. does not teach that the gate length of the gate electrode and the impurity concentration are a result-effective variable. Thus, the rejection of claims 7 and 8 as being obvious over Hidaka et al. is in error.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action are respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,



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